Question Bank

Subject : Digital Circuits And Fundamental Of Microprocessor

BEENE404T

BE IV Semester Electronics

Unit I: Combinational Circuits

Standard representations for logic functions, k map representation of logic functions (SOP & POS forms), minimization of logical functions for min-terms and max-terms (upto 4 variables), don't care conditions, Design Examples: Arithmetic Circuits, BCD - to – 7 segment decoder, Code converters.

Que1. Simplify using K-map and realize using gates.

i. $f(A, B, C, D) = \sum m(0, 1, 4, 5, 9, 11, 14, 15) + \sum d(10,13)$.

ii. $f(w, x, y, z) = \prod M(1, 3, 9, 10, 11, 14, 15)$

Que2. Convert the following expression into standard pos form.

$f(A, B, C) = \overline{A}B + BC + A\overline{C}$.

Que3. Design binary to gray code converter (3 bit binary).

Que4. Implement the function in standard SOP form

$f = AB + A\overline{C} + C + AD + A\overline{B}C + ABC + \overline{B}C$

Que5. Simplify the following functions using K-map.

i) $f(A,B,C,D) = \sum m(0,1,5,9,11,14,15) + d(10,13)$

ii) $f(PQRS) = \pi m(1,3,9,10,11,14,15) + d(2,7)$

Que6. Design Binary to Gray Code converter and implement the circuit using logic gates.

Que7. Explain standard SOP and standard POS forms of Boolean equation. Also explain Min terms and Max terms concept.

Que8. Minimize the function and implement using NAND logic

$f(A, B, C, D) = A\overline{B}CD + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}\,\overline{D} + ABCD$

Que9. Use K-MAP to solve the following. Also implement the result using universal gate logic only.

i) $f(A, B, C, D) = \sum m(0, 1, 4, 6, 7, 11, 12, 13, 15) + d(3, 10)$

ii) $F(P, Q, R, S) = \prod M(1, 4, 8, 10, 12, 13, 15) \cdot D(2, 11)$

Que10. Design a code converter which will convert 3 bit binary number applied at the input into equivalent gray code.

Que11. Realize the following functions using K-maps.

a) $f(W, X, Y, Z) = \Sigma m(0, 2, 3, 5, 7, 11, 12, 15) + d(4, 6, 13)$

b) $f(P, Q, R, S) = \pi M(1, 3, 4, 6, 7, 9, 10, 13, 15) + d(8, 12)$

Que12. Design a Gray to Binary (4 bit) converter using suitable gates.

Que13. State and explain Demorgan's Law.

Que14. Simplify the following function using K-map.

i. $f(A, B, C, D) = \sum m(0, 2, 5, 9, 15) + \sum d(6, 7, 8, 10, 12, 13)$.

ii. $f(w, x, y, z) = \prod M(1, 4, 5, 6, 11, 12, 13, 14, 15)$

Que15. Express the function in standard SOP form

$F = \overline{A} + A.B + B.\overline{C}$

Que16. Express the function in standard POS form.

$F = (A + B)(A + C)(B + \overline{C})$

Que17. Design a BCD to seven segment decoder for common cathod configuration.

Unit II :Logic Circuit Design

Adders and their use as substractor, look ahead carry, ALU, Digital Comparator, Parity generators/checkers, Static and dynamic hazards for combinational logic. Multiplexers and their use in combinational logic designs, multiplexer trees, Demultiplexers, Encoders & Decoders .

Que1. Design and implement full adder from two half adders and one OR gate. Draw the logic circuit and give its truth table.

Que2. Design a BCD to 7 segment decoder circuit.

Que3. Design a 3 bit odd parity generator and implement with NAND gates.

Que4. Implement 16:1 multiplexer using 4: 1 multiplexers.

Que5. Implement the following function using 8: 1 multiplexer.

$F = \sum m(0, 1, 2, 3, 11, 12, 14, 15)$.

Que6. Design a magnitude comparator to compare the magnitude of two, 2 bit binary numbers and draw the logic diagram.

Que7. Implement the following using 3:8 decoder circuit.

$F_1 = \sum m(0, 1, 2, 4)$.

$F_2 = \sum m(4, 5, 6, 7)$.

Que8. Draw and explain the Arithmetic and Logic Unit. (ALU)

Que9. Design a BCD to seven segment decoder for common cathode configuration.

Que10. Design 1:32 demultiplexer using 1:8 demultiplexers & 1:4 DEMUX.

Que11. Implement the following function using 8:1 multiplexer

$F(A, B, C, D) = \sum m(0, 2, 4, 5, 7, 9, 12, 15)$

Que12. Design a decimal to BCD encoder and explain.

Que13. Explain how a Full Adder is constructed using Half Adder Circuits.

Que14. What do you mean by hazard? Explain various hazards for combinational circuits.

Que15. Design a 32 : 1 MUX using 2 : 1 MUX.

Que16. What is the difference between encoder & decoder? Explain priority encoder

Que17. How will you implement full subtractor using two half subtractors and one or gate? Explain?

Que18. Design a ckt which detects even parity of a 4 bit binary no.

Que19. Implement the following function using 4:1 multiplexer.

$F(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$

Que20. Design the 3 bit priority encoder and implement it.

Unit III: Sequential Logic Design

1 Bit Memory Cell, Clocked SR, JK, MS J-K flip flop ,D and T flip-flops. Use of preset and clear terminals, Excitation Table for flip flops. Conversion of flip flops.

Que1. What do you mean by Race around condition in JK flip flop? How this condition can be overcome?

Que2. Convert D flip flop to T flip flop.

Que3. Convert T flip flop to JK flip flop.

Que4. Convert SR to JK flip flop.

Que5. Convert JK flip flop to T flip flop.

Que6. Convert T flip-flop to S-R flip-flop

Que7. Convert SR to T flip flop.

Que8. Draw the logic diagram of JK flip flop using NAND gate and explain its working. Give the characteristics equation of JK flip flop?

Que9. Explain how latch can be used as one bit memory cell.

Que10. Explain the function of preset and clear terminal of flip-flop.

Que11. What is master slave J-K flip flop? How is race around condition eliminated by using this configuration.

Que12. Explain the operation of T and D flip flop using NAND gate.

Que13. What is master slave J-K flip flop ? Explain with neat diagram. Also show it NAND logic implementation.

Que14. Explain different types of trigger used in digital circuits.

Que15. What do you mean by race around condition? Clearly explain how it can be avoided.

Que16. Explain S. R. flip flop using NAND Gates only.

Que17. What is master slave flip-flop? Give logic diagram of JK master- slave flip-flop using NAND gates. Explain its working.

Que18. Explain the difference between truth table and excitation table of flip-flop.

Que19. Draw the logic diagram of D flip-flop using NAND gate.

Unit IV : Application of Flip flops:

Registers, Shift registers, Counters (ring counters, twisted ring counters),Sequence Generators, ripple counters, up/down counters, synchronous counters, lock out, Clock Skew

Que1. Explain the operation of Johnson's counter with waveforms.

Que2. Explain the working of 4 bit left-shift register with neat sketch and explain.

Que3. Design a synchronous lock free counter using D flip flop that passes through.

$$S_0 \rightarrow S_2 \rightarrow S_4 \rightarrow S_5 \rightarrow S_6$$

Que4. Explain the difference between asynchronous and synchronous counters.

Que5. Design and draw a 3 bit synchronous counter which goes through the following states: $S_1 \rightarrow S_3 \rightarrow S_5 \rightarrow S_7$

Que6. Draw and explain 4 bit Ripple counter with waveform.

Que7. Draw the logic diagram of 4 bit serial In serial Out shift register and explain its operation.

Que8. Write short note on Twisted Ring counter.

Que9. Design and draw a 3-bit synchronous counter which passes through the following states. $S_1 \rightarrow S_6 \rightarrow S_4 \rightarrow S_3$

Que10. Draw and explain 4-bit Ripple counter with waveforms.

Que11. Draw the logic diagram of 4 bit bidirectional shift register and explain its working.

Que12. Explain twisted Ring counter with neat block diagram.

Que13. Differentiate between Synchronous & Asynchronous counters. What do you mean by a modulus of counter?

Que14. Design a modulo - 10 synchronous counter using suitable flip flop.

Que15. Explain universal shift register circuit.

Que16. Design a 3 bit up / down asynchronous counter circuit.

Que17. Design a synchronous counter for

$$S_4 \rightarrow S_6 \rightarrow S_7 \rightarrow S_3 \rightarrow S_1$$

Avoid lockout condition. Use J-K flip-flop for design.

Unit V: Digital Logic Families

Classification of logic families , Characteristics of digital ICs-Speed of operation , power dissipation, figure of merit, fan in, fan out, Comparison table of Characteristics of TTL, CMOS, ECL, RTL, I^2L, DCTL.
Classification and characteristics of memories: RAM, ROM, EPROM, EEPROM, NVRAM, SRAM, DRAM, expanding memory size, Synchronous DRAM (SDRAM), Double Data Rate SDRAM, Synchronous SRAM, DDR and QDR SRAM, Content Addressable Memory
Programmable logic devices: Detail architecture, Study of PROM, PAL, PLA, Designing combinational circuits using PLDs.

Que1. Explain the operation of TTL as a NAND gate.

Que2. Explain the following with respect to digital IC'S.

i) Speed of operation ii) Fan out iii) Fan in

iv) Figure of merit. v) Power dissipation. vi) Noise margin

Que3. Write a short note on Programmable Logic Array (PLA).

Que4. Explain the classification and characteristics of semiconductor memory.

Que5. Explain content addressable memory.

Que6. Write a short notes on PAL Device.

Que7. Write a short notes on SRAM Memory.

Que8. Write a short notes on TTL family.

Que9. Write a short notes on EPROM Memory

Que10. Compare TTL and CMOS logic families with at least five points.

Que11. Write short notes on Types of Integrations.

Que12. Show comparison table of characteristics for TTL, CMOS, ECL & RTL, I^2L.

Que13. Explain how a memory is interfaced with microprocessor.

Que14. Differentiate between static & dynamic RAM.

Que15. Write a short notes on RAM Memory

Que16. Write a short notes on ROM Memory

Que17. Write a short notes on EEPROM Memory

Que18. Explain the characteristics of Digital IC's.

Que19. Explain the operation of TTL as a NAND gate.

Unit VI: Fundamental of Microprocessor

Introduction to microprocessor, Architecture of 8085 microprocessor, Addressing modes, 8085 instruction set, Interrupts, Concept of assembly language programming.

Que1. Explain Architecture of microprocessor 8085 in detail.

Que2. Explain addressing modes of microprocessor 8085.

Que3. Explain interrupt structure of microprocessor 8085 in detail.

Que4. Explain the following.

i. LDA 16 bit Addr. ii) DAA.

Que5. Draw and explain the internal block diagram of 8085, Microprocessor.

Que6. Explain the flag register of 8085 Microprocessor.

Que7. What do you mean by addressing mode? Explain all addressing mode of 8085.

Que8. Explain the following instructions of 8085 Microprocessor.

i) MVI A, 11 H;

ii) DAA;

iii) RST 7.5;

iv) CALL 1000H

Que9. Explain various addressing modes of 8085 microprocessor. Also give one example for each one.

Que10. Explain the following instructions of 8085 microprocessor.

i) MOVA, M ii) DAA

iii) CALL 1000H iv) XCHG

Que11. Write an assembly language program to add two BCD numbers and save the maximum possible result from memory location 2050 H.

Que12. Explain the classification of instruction set of 8085 microprocessor with example.

Que13. Write a program to arrange 10 bytes of data in ascending order.

Que14. Explain following pairs.

a) X1 & X2 b) READY c) ALE d) $\overline{\text{INTA}}$