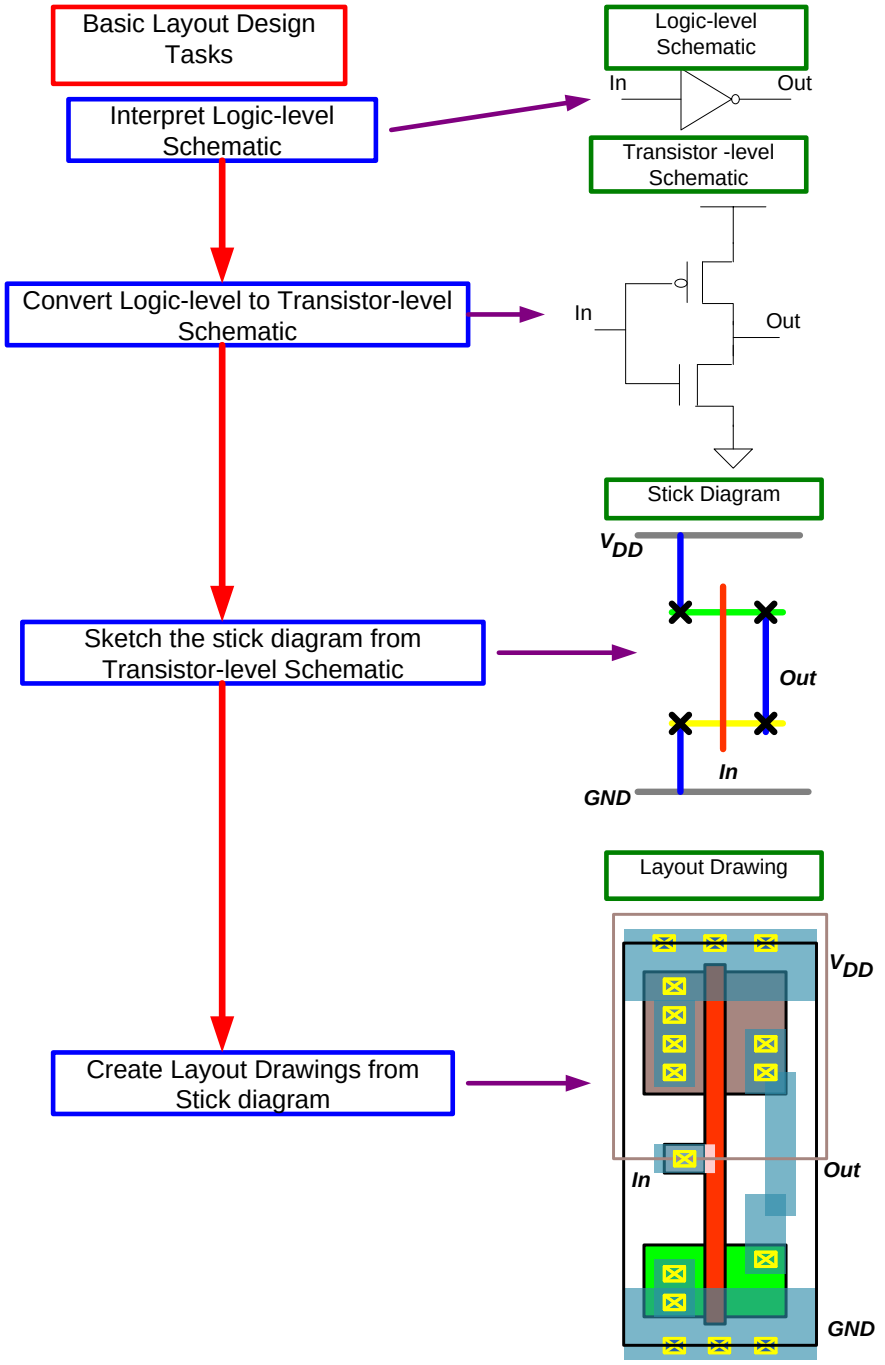
Layout I (Stick Diagram)

EMT 251 Introduction to IC Design

Steps for Layout Design

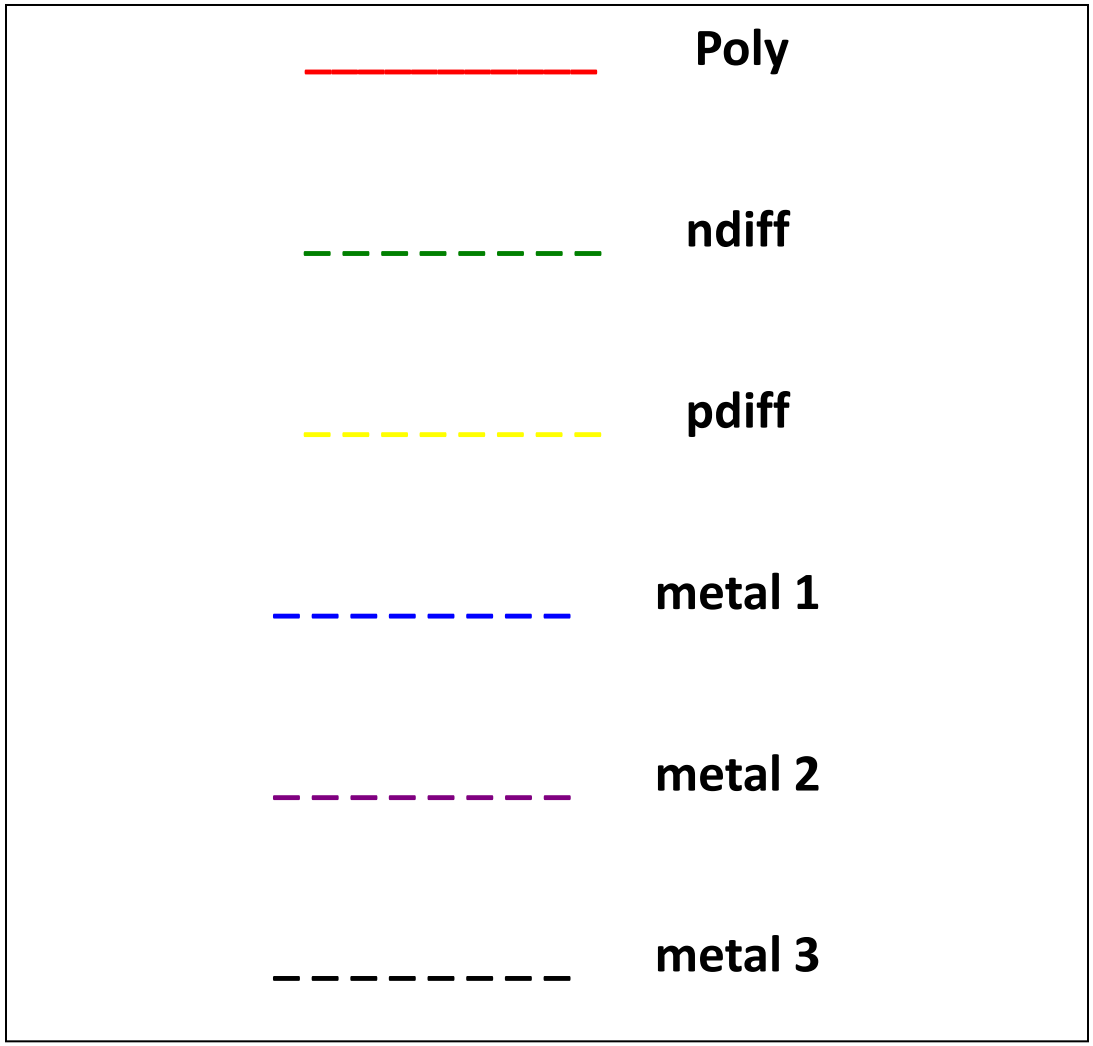


Stick Diagram

- A stick diagram is a graphical view of a layout or cartoon of a chip layout.
- It is easy to draw because it does not need to be drawn to scale.
- The differences between stick diagram and layout are caused by zero-width line and zero area transistor in stick diagram.
- It is because it does not show exact placement, transistor sizes, wire lengths, wire widths and tub boundaries. But it can be as guidance to move the transistor or vias or reroute the wires to minimize the used of the wire. It can be draw with color pencil or dry-erase markers.

Stick Diagram

- Layout construct from shapes like rectangular or squares meanwhile stick diagrams represents relative positions of transistors with rectangular or mark (X) as component symbols and lines as wires.
- The wires symbol can be in various colors such as red for poly, green for n-diffusion, yellow for p-diffusion and blue for metal1 as shown in Figure (next slide).
- Otherwise, the wire also can be drawing in different types of lines such as straight line, dotted line, short dashed line and etc.



The wires symbol

Stick Diagram

- There are a few simple rules for constructing stick diagram to ensure the stick diagram is corresponding to a feasible layout.
- First, the wires must be drawn in horizontal or vertical lines and two wires.
- Second, two wires segments on the same layer which cross are electrically connected so vias is used to connected wires that do not interact.
- Table (next slide) shows the complete rules of possible interactions between layers which show that how wires on different layers allowed to cross each other.
- This table is derived from the manufacturing design rule

Rules for possible interactions between layers (connection rules)

metal3	metal2	metal1	Poly	ndiff	pdiff	
short	open	open	open	open	open	**metal3**
	short	open	open	open	open	**metal2**
		short	open	open	open	**metal1**
			short	n-type	p-type	**Poly**
				short	illegal	**ndiff**
					short	**pdiff**

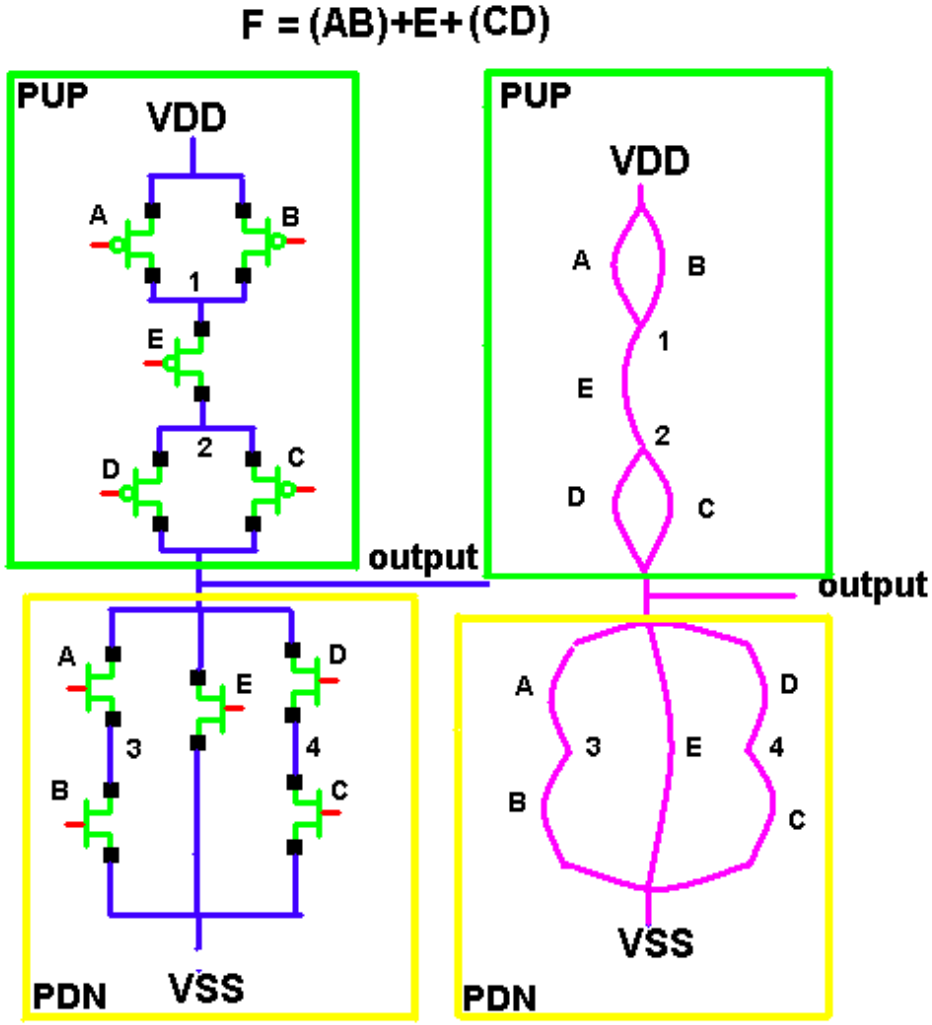
Stick Diagram Steps

1) Construct a logic graph of the schematic.

- Figure 8.1 shows the schematic and graph for equation . From this figure, **identify each transistor by a unique name** of its gate signal (A, B, C, D, and E). Then **identify each connection to the transistor by a unique name** (1, 2, 3 and 4).

- Figure 8.1 - (next slide)

Fig 8.1: Schematic & graph

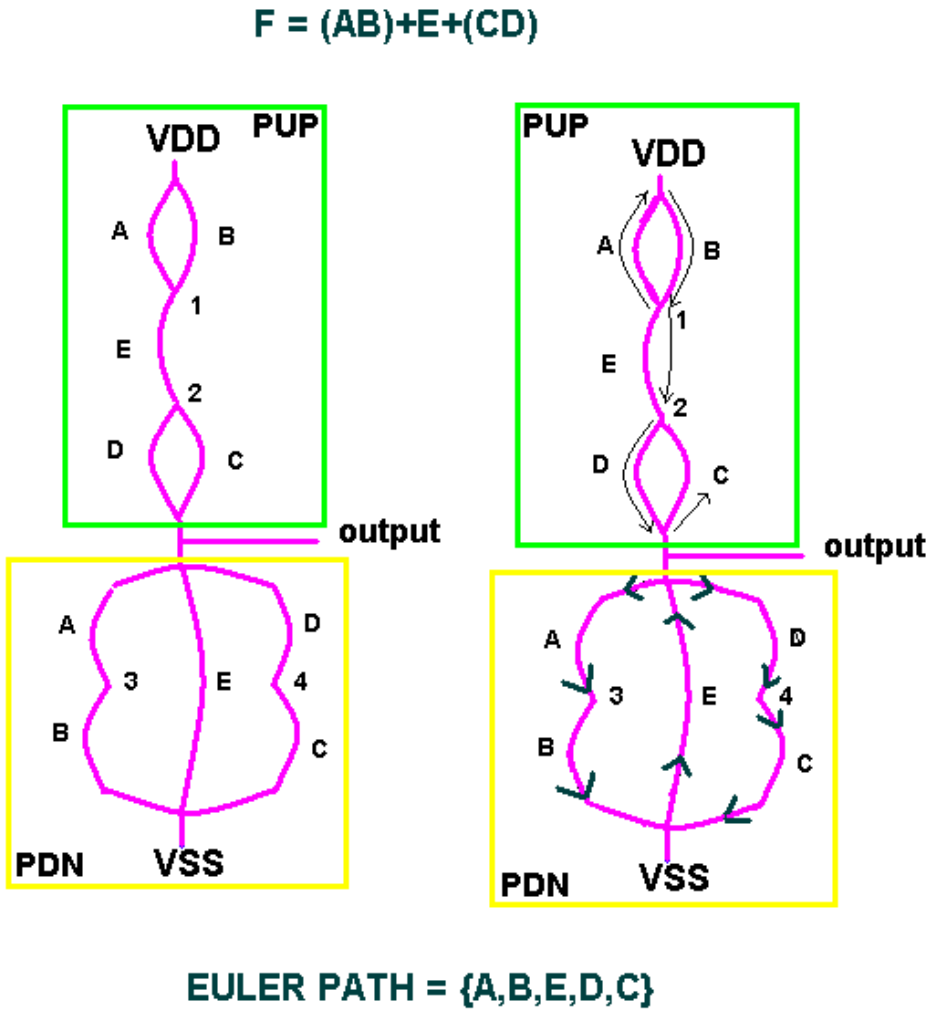


Stick Diagram Steps

2) Construct one Euler path for both the Pull up and Pull down network

- Figure 8.2 shows the example of Euler Path. Euler paths are defined by a path the traverses each node in the path, such that each edge is visited only once. The path is defined by the order of each transistor name. If the path traverses transistor A then B then C. Then the path name is {A, B, C}. The Euler path of the Pull up network must be the same as the path of the Pull down network. Euler paths are not necessarily unique. It may be necessary to redefine the function to find a Euler path.

Fig 8.2: Euler Path



Stick Diagram Steps

3) Sketch the lines as references

- Then time to sketch the stick diagram after found the Euler Path as in Figure 5.13. There are a few lines that must be sketch as reference before connect the wire for the schematic. The lines are:
- Sketch two green lines horizontally represent the NMOS and PMOS devices.
- Sketch the number of inputs (5 in this example) vertically across each green strip. These represent the gate contacts to the devices that are made of Poly.
- Surround the NMOS device in a yellow box to represent the surrounding Pwell material.

Stick Diagram Steps

- Surround the PMOS device in a green box to represent the surrounding Nwell material.
- Sketch a blue line horizontally, above and below the PMOS and NMOS lines to represent the Metal 1 of VDD and VSS.
- Label each Poly line with the Euler path label, in order from left to right.
- Place the connection labels upon the NMOS and PMOS devices.

Stick Diagram Steps

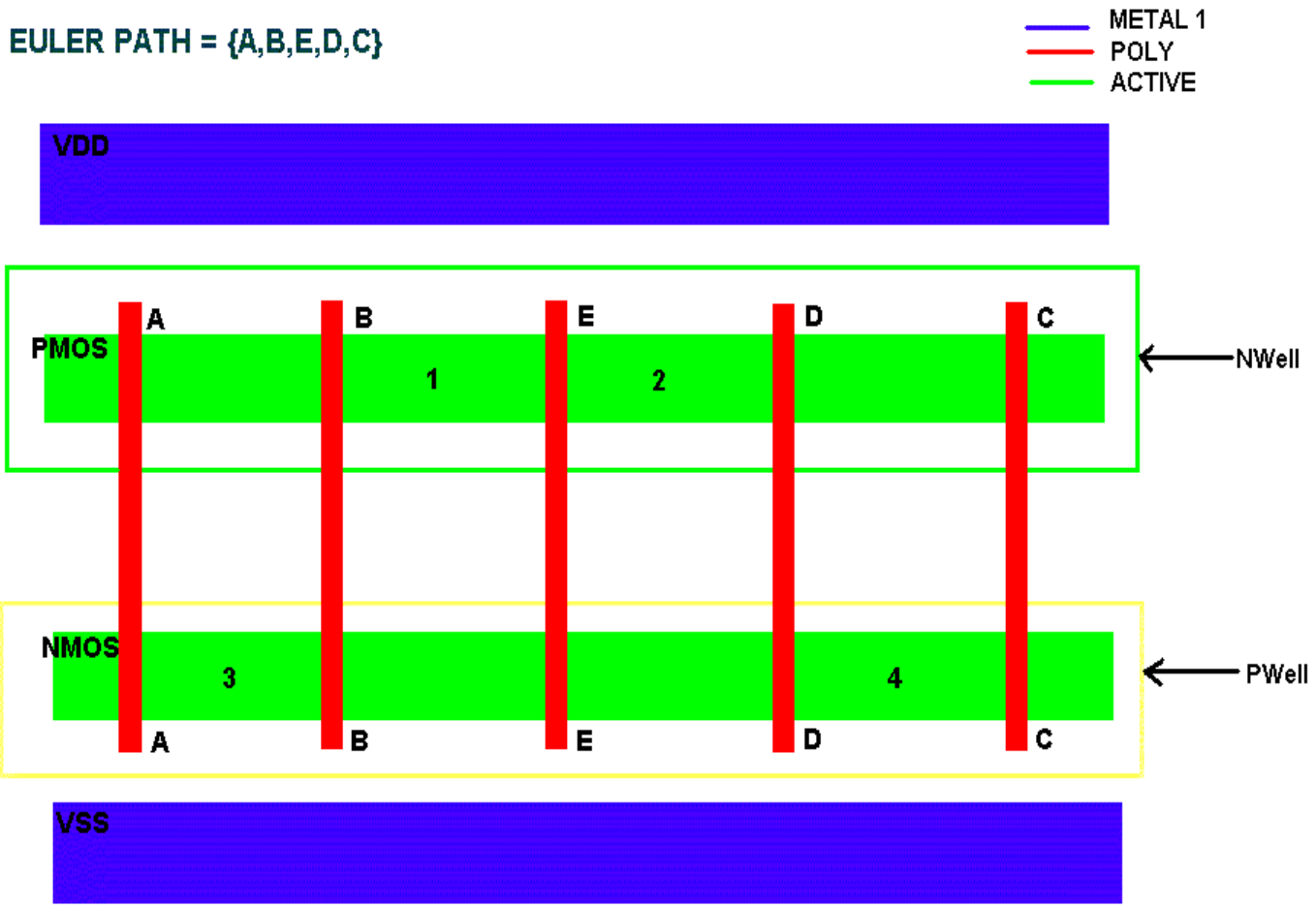
4) Labeling the connection

- As in Figure 8.3 the connection labels are 1, 2, 3, and 4.
  - Connection 1 is the node that lays between the PMOS transistors A, B and E. The Euler path defines the transistor ordering of {A, B, E, D, C} therefore, transistor B is physically located beside transistor E. The connection of label 1is placed between the transistors B and E. Later, Metal 1 connection will route from the drain of transistor A to the connection label of 1.

Stick Diagram Steps

- Connection 2 is the node that connects the PMOS transistors of E, D, and C. Since the Euler path places transistors E and D next to each other, place the connection label between these two. Later, we will route a Metal 1 strip from the source of C to connection label 2.
- Connection label 3 lies between the NMOS transistors of A and B.
- Connection label 4 lies between the NMOS transistors of D and C.

Fig 8.3: Connection label layout



Stick Diagram Steps

5) Placing the VDD, VSS and outputs

- Then place the VDD, VSS and all output names upon the NMOS and PMOS devices as in Figure 8.3.
  - This signal is connected to the PUP device through a node located between transistors D and C. Meanwhile the other three transistors A, E and D share the connection at the PDN.
  - The Euler graph connects transistors E and D together so an output connection will be located there. Transistor A has one remaining contact that is unused, so the output label is placed at that position.

Stick Diagram Steps

- The VDD is located upon the PMOS device at the node shared between transistors A and B. In the meantime, VSS is located upon the NMOS device at a node that is shared between transistors B, E and C.

- The Euler path places transistors B and E together so place a VSS label between the transistors there. Transistor C has one remaining contact that is unused. Place a VSS label there.

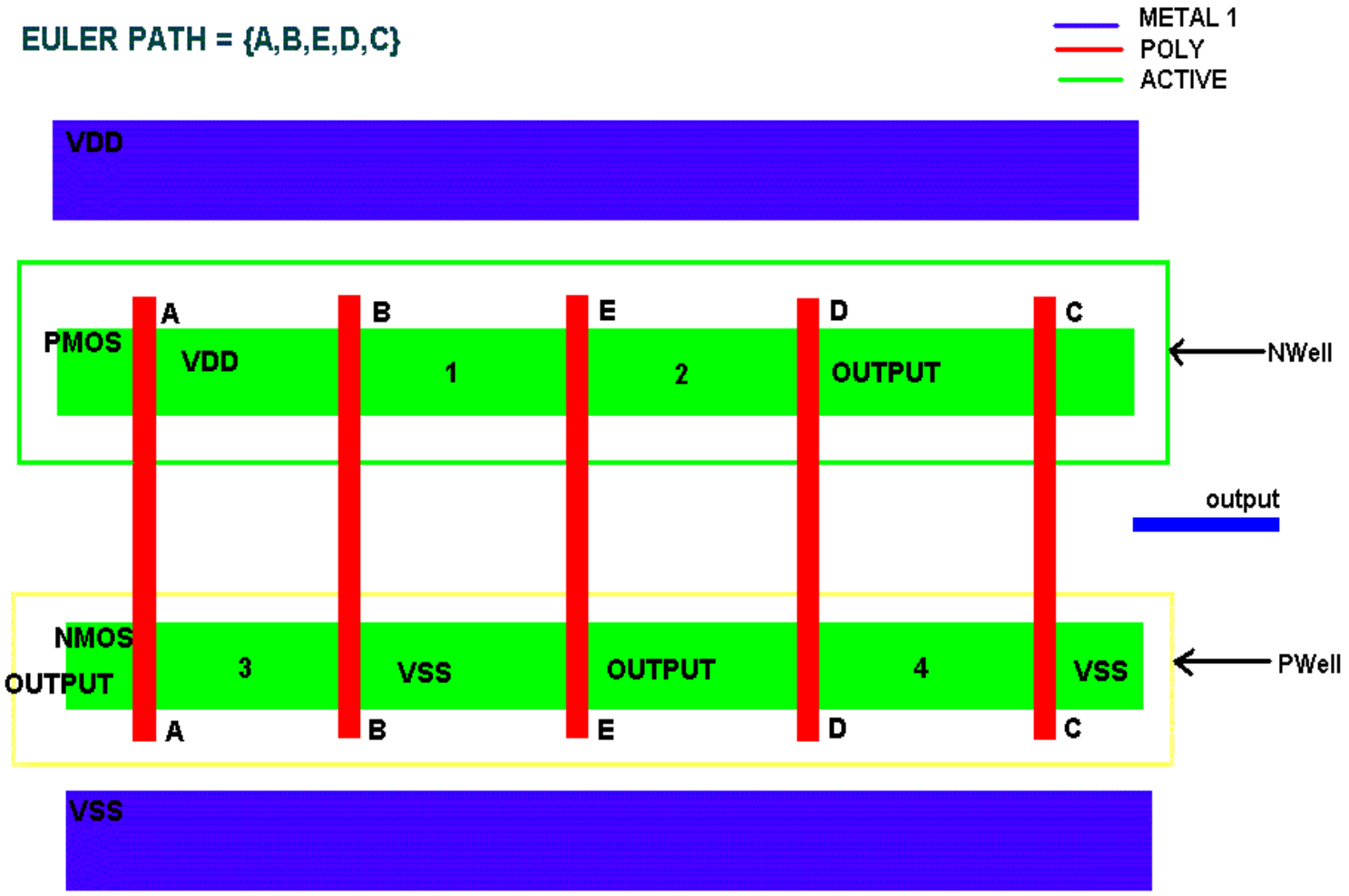
Stick Diagram Steps

6) Blue line for output

- After that, place a blue line on the diagram to represent the output metal one material as in Figure 8.4.

- *Note: this line may have to be moved around depending on how the diagram connections will lay out.*

Fig 8.4:VDD,VSS and Output Labels



Stick Diagram Steps

7) Interconnection

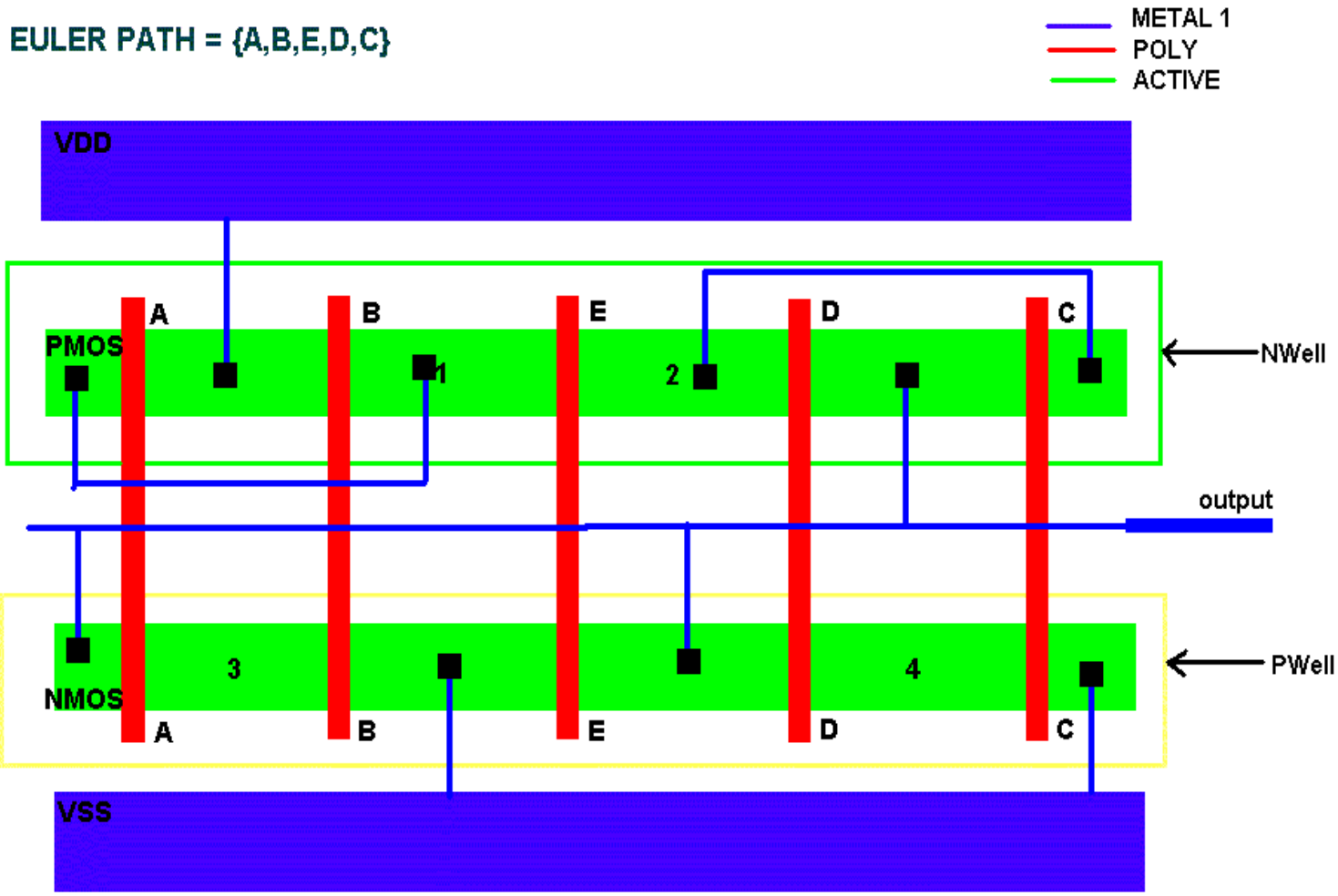
- The last part and very interesting part is to interconnect the device and to find the best routing as in Figure 8.5.
  - Poly and Metal 1 can overlap.
  - Avoid routing signals that are side by side for long lengths. This adds capacitance to the device.
  - Avoid all interconnect overlap if possible. This adds capacitance to the device. Strive for simplicity. This will later provide the smallest and fastest devices.

Stick Diagram Steps

- There is other option to use Poly, Metal 2, and even Active to interconnect the device. But there are disadvantage such as:
  - Poly and especially Active adds resistance to you device.

- Avoid using Metal 2 if possible. Metal 2 is another layer to your device that you will probably need in the next hierarchy up.

Fig 8.5: Stick Diagram, Interconnected



Summarize

- There are seven steps to make the stick diagram, which are:
  - Construct a logic graph of the schematic.
  - Construct one Euler path for both the Pull up and Pull down network
  - Sketch the lines as references
  - Labeling the connection
  - Placing the VDD, VSS and outputs
  - Blue line for output
  - Interconnection

Exercise 1

- Construct stick diagram for equation below:
  - F = (A+B) . CD
  - Other exercises?