K.D.K. COLLEGE OF ENGINEERING

Department of Electronics Engineering

B. **E. Seventh Semester Electronics Engineering**
Subject : Advanced Digital System Design

Subject Code : BEENE704P | **College Assessment : 25 Marks**
Duration : 2 Hr. | **University Assessment : 25 Marks**

List of Experiments:

1. Design of basic logic gates using VHDL.
2. Design of Half Adder using data flow style and full adder using structural style of modeling.
3. Design of Multiplexer / Demultiplexer using VHDL.
4. Using a case statement, write VHDL code for 3:8 Decoder.
5. Design of Priority encoder using structural style of modeling.
6. Design of BCD to Seven Segment Decoder using case statement.
7. Design of behavioral VHDL code for D Flip Flop.
8. Using GENERATE statement Design of behavioral VHDL code for 4-bit shift register.
9. Design of VHDL code for sequence detector using Mealy FSM.
10. Design of VHDL code for sequence detector using Moore FSM.
11. Using Data flow code write VHDL code for 1-bit, 2-bit comparator.

Signature of the Lab. Incharge

Signature of the Subject Teacher